V-BAND MONOLITHIC POWER MESFET AMPLIFIERS*

G. Hegazi, H-L. Hung, F. Phelleps, L. Holdeman, A. Cornfeld,
T. Smith, J. Allison, and H. Huang

COMSAT Laboratories
22300 Comsat Drive
Clarksburg, Maryland 20871-9475

ABSTRACT

Monolithic GaAs power amplifiers have been developed at V-band. A single-stage amplifier provided over 4-dB gain from 50 to 56 GHz, with output power of 95 mW and a power-added efficiency of 11 percent at 55 GHz. A cascaded amplifier achieved 16.2-dB gain and output power of 85 mW. These results may represent the highest power/gain yet reported from V-band power monolithic microwave integrated circuits (MMICs).

INTRODUCTION

Future millimeter-wave systems for intersatellite communications and electronic warfare applications will require power amplifiers in the 50- to 70-GHz frequency range. Recently, Kim et al. [1] reported the results of a GaAs metal semiconductor field-effect transistor (MESFET) monolithic amplifier delivering 25 mW with 8-percent efficiency at 54 GHz.

Smith et al. [2] reported the device performance of a discrete modulation doped field-effect transistor (MODFET) with 50-mW output power, 3-dB gain, and 11-percent efficiency at 60 GHz. InGaAs/GaAs pseudomorphic MODFET devices have also demonstrated power of 20 mW at 60 GHz [3].

This paper describes new results from GaAs MESFET MMICs operating in V-band. An optimized device structure together with computer-aided design (CAD) programs developed in house resulted in the use of MESFETs with larger gate width than those previously reported, achieving high-output-power monolithic circuits from the initial design. Built-in, DC-blocking capacitors and bias networks have allowed the cascading of these MMICs, providing usable power gain with stable operation. The results presented here may represent the highest gain/power performance yet reported at 55 GHz.

MESFET Design

MESFET design and optimization was performed with a computer device modeling and load pull program [4] developed in house. The program first generates a bias-dependent equivalent circuit and DC characteristics of the MESFET based on its physical and material parameters and geometrical dimensions.

The two quantities calculated by the computer program and related to the MESFET output power capability are the knee voltage 'V_k', which is the drain voltage at the onset of drain current saturation, and the maximum drain current, I_{max}, that flows in the MESFET when the gate is slightly forward biased (which is the case in large-signal operation).

The program then uses the bias-dependent equivalent circuit, breakdown voltage, V_{bd}, V_k, and I_{max} to calculate the FET output linear power, linear power gain, and power-added efficiency. This is achieved by solving the FET-equivalent circuit to find all the node voltages with the following two constraints: 1) the voltage between the drain and gate cannot exceed V_{bd} minus V_k; 2) the drain current cannot exceed I_{max}. After the node voltages are solved for, the input and output powers are calculated and the input assigned a certain load impedance. A built-in optimization routine varies the load impedance of the FET and solves the voltage and current at each node of the equivalent circuit for a given load, until a load impedance is found that maximizes the output linear power. The load may also be optimized for maximum power-added efficiency or maximum power gain.

This program allows a parametric study of the device/circuit performance by changing device parameters such as channel doping, height, and gate length. Thus, the FET can be optimized to provide the desired output power and power-added efficiency for a given frequency. It was found that as the frequency increases, the channel doping should increase while the channel height should decrease. The gate length-to-channel height ratio (L/a) should be kept above unity to maintain low output conductance of the FET.

In this power amplifier design, the FET consists of 12 gate fingers, with a unit gate width of 25 μm, to provide a total gate width of 0.3 mm. The sub-half-micron gate was recessed down to an appropriate channel height to achieve a pinch-off voltage of 2 V. This gate recess reduces the gate and drain resistances. The channel doping was selected to be 5×10^{17} cm^{-3}.

*This paper is based on work performed at COMSAT Laboratories under the sponsorship of the Communications Satellite Corporation.

0149-645X/88/0000-0409$01.00 © 1988 IEEE

The theoretically generated contours of constant power gain and constant output power for the designed 0.3-mm gate width MESFET are shown in Figure 1. The maximum linear output power of the MESFET is seen to be 90 mW when matched to the load of 14.2 + j27.29 Ω, with a corresponding gain of 5 dB at 55 GHz.

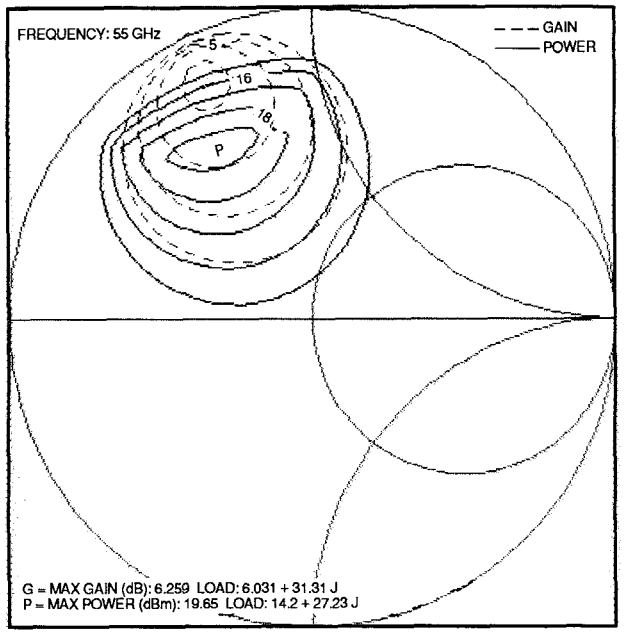


Figure 1. Impedance Contours for Constant Gain and Constant Output Power of the 0.3-mm MESFET at 55 GHz

MMIC Design

Distributed element matching was employed in the design of the power chip to minimize circuit loss. Shunt inductances were implemented as stubs shorted to ground through 4-pF MIM capacitors and via-holes, while shunt capacitances were implemented as open stubs. The output matching circuit presents the optimum load for the FET to deliver maximum output power. The input matching circuit conjugate matches the FET input impedance when loaded with the output matching circuit, and was optimized for bandwidth and gain flatness. MIM DC-blocking capacitors (2 pF) were also integrated in the circuit, so that amplifiers could be directly cascaded.

The mask was designed so that individual amplifier circuits could be cascaded and/or combined by interconnecting them with e-beam at the gate metallization level, thus providing higher gain and power.

Fabrication

The MMICs were fabricated using e-beam direct writing gate and photolithography similar to the process previously reported [5]. Vapor-phase epitaxy was employed to grow a buffer layer and n and n^+ layers on the semi-insulating substrates. Metal-insulator-metal capacitor base metal was defined by lifting off Ti/Pt/Au. The dielectric layer was 2500-Å thick Si_3N_4, and the top plate metallization was Ti/Au at a thickness of 2 μm. Through-substrate via-holes were defined by infrared (IR) and spray etching techniques to provide low-inductance grounding for the FET sources and the shunt capacitors.

Measured Results

The monolithic amplifiers were measured in a WR-15 waveguide system using a pair of finline waveguide-to-microstrip transitions. The finline patterns, which were printed on both sides of a 5-mil fused silica substrate, consist of two antipodal exponential tapers that transform the impedance of the waveguide into the 50-Ω impedance of the microstrip line. The E-field of the empty waveguide is rotated 90° as it passes through the tapers to a balun section, which prevents reflections of unbalanced modes from the microstrip to the waveguide. Serrations were printed on the substrate to act as an RF choke at the gap between the two halves of the waveguide, thus preventing mechanical contact between the upper waveguide half and the substrate. The amplifier assembly, with two waveguide-to-microstrip transitions and an MMIC on the center block, is shown in Figure 2. The measured performance of two back-to-back transitions is shown in Figure 3. Insertion loss and return loss of one waveguide-to-microstrip transition were 0.5-0.7 dB and better than 18 dB, respectively, from 50 to 60 GHz.

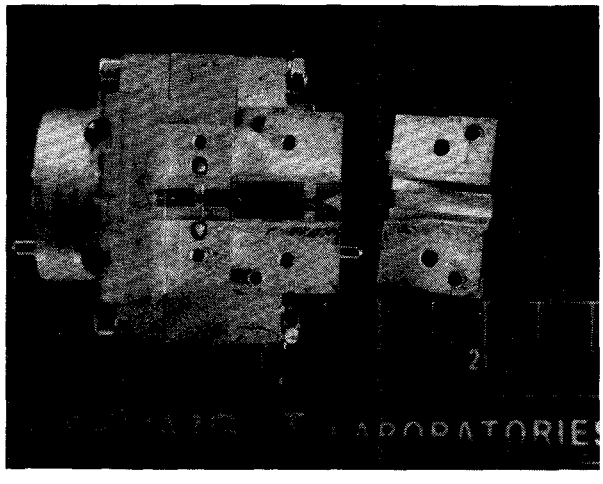


Figure 2. Amplifier Assembly Showing Waveguide-to-Microstrip Transitions

Figure 4 is a photograph of the power MMIC. The measured small-signal gain was over 4 dB from 50 to 56 GHz, as shown in Figure 5a. Figure 5b shows the P_{out} vs P_{in} curve at 55 GHz. A power level of 95 mW and a power-added efficiency of 11 percent were obtained at that frequency.

MMIC modules were cascaded to achieve higher power gain, and stable operation was observed. Figure 6 shows the performance of the four-stage amplifier. Better than 16-dB power gain was measured in the 52- to 57-GHz frequency range. At 55 GHz, 85-mW output power was obtained.

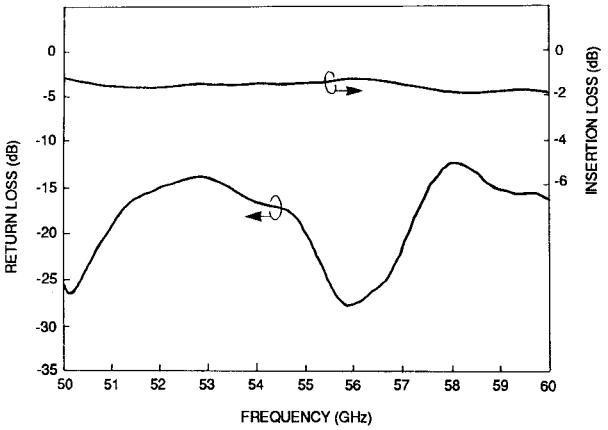
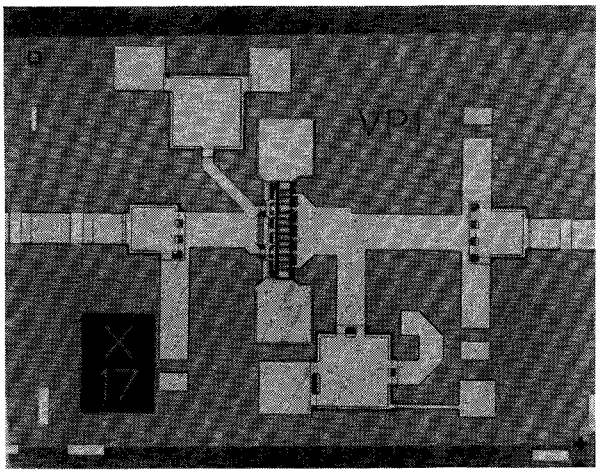
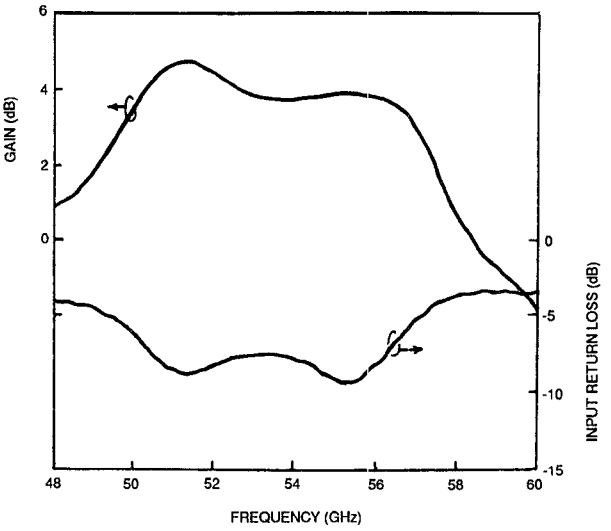


Figure 3. Performance of Two Antipodal Finline Waveguide-to-Microstrip Transitions

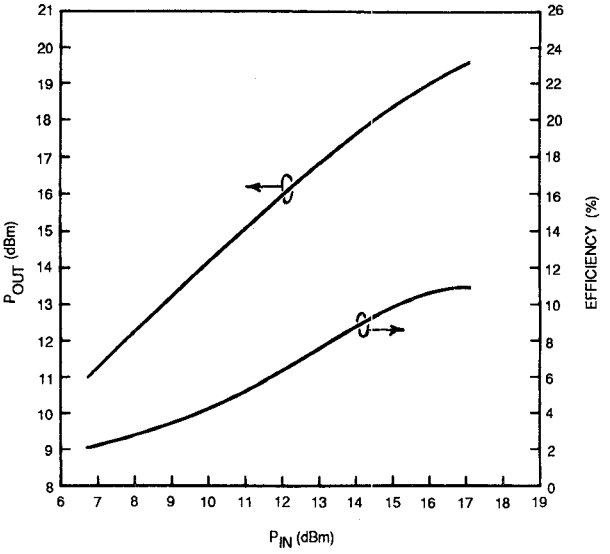


MMIC Chip 30 mil x 40 mil (0.75 x 1.0 mm)

Figure 4. V-Band Power MMIC

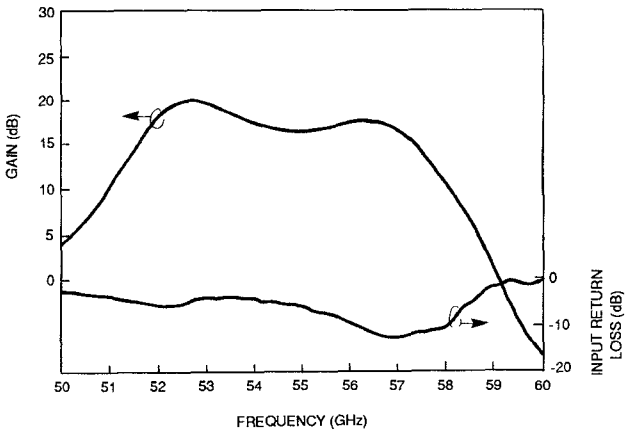


(a) Gain and Input Return Loss vs Frequency

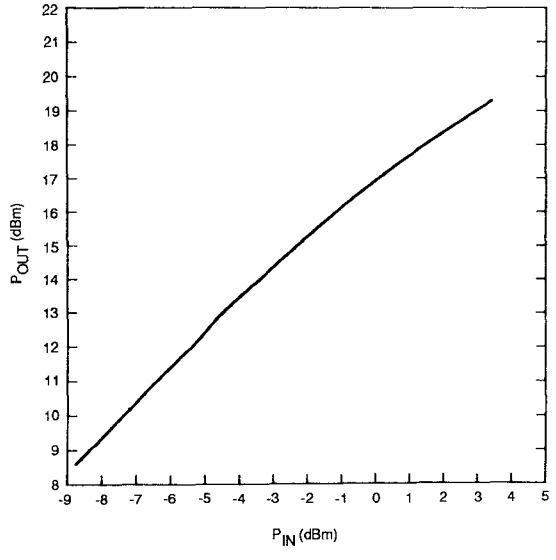


(b) Output Power and Power-Added-Efficiency vs Input Power

Figure 5. Measured Small-Signal Gain and P_{OUT} vs P_{IN} Curve



(a) Frequency Response



(b) Output Power vs Input Power

Figure 6. Performance of Four-Stage MMIC Amplifier

CONCLUSIONS

V-Band GaAs monolithic power amplifiers using a 300-μm gate width MESFET have demonstrated output power of near 100 mW at 55 GHz. Accurate device/circuit modeling has also resulted in stable multistage amplifiers, providing power gain exceeding 16 dB. The capability of these power amplifiers and the low-noise MMICs reported in [6] has demonstrated the potential of MESFET MMICs for applications in satellite and EW systems.

ACKNOWLEDGMENTS

The authors would like to acknowledge the efforts of J. Kearney for mask layout, E. Carlson for on-wafer device characterization, and J. Singer for RF assembly and testing.

REFERENCES

[1] B. Kim, et al., "Millimeter-Wave Monolithic GaAs Power FET Amplifiers," Microwave Journal, March 1987, pp. 153-163,.

[2] P. Smith, et al., "Advances in HEMT Technology and Applications," IEEE International Microwave Symposium, Digest, May 1987, pp. 749-752.

[3] T. Henderson, et al., "Microwave Performance of a Quarter-Micrometer Gate Low-noise Pseudomorphic InGaAs/AlGaAs Modulation-Doped Field Effect Transistor," IEEE Electron Device Letter, Vol. EDL-7, No. 12, December 1986, pp. 649-651.

[4] H.-L. Hung, G. Hegazi, K. Peterson, and H. Huang, "Design and Performance of GaAs Power MESFET Amplifiers at K- and Ka-Band," scheduled for publication in the Microwave Journal, 1988.

[5] H.-L. Hung, et al., "Ka-Band Monolithic Power Amplifiers," IEEE Microwave and Millimeter-Wave Monolithic Circuit Symposium, Digest, June 1987, pp. 97-100.

[6] H.-L. Hung, et al., "60-GHz GaAs MMIC Low-Noise Amplifiers," scheduled for presentation at IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1988.